

# MN39143AT

## Diagonal 6.0 mm (type-1/3) 410k-pixel CCD Area Image Sensor

### ■ Overview

The MN39143AT is a 6.0 mm (type-1/3) interline transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal readout. The electronic shutter function has made an exposure time of 1/10000 seconds possible. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 403 920 pixels (816 horizontal × 495 vertical) and provides stable and clear images with a resolution of 550 horizontal TV-lines and 350 vertical TV-lines.

| Part Number | Size             | System | Color or B/W |
|-------------|------------------|--------|--------------|
| MN39143AT   | 6.0mm (type-1/3) | EIA    | B/W          |

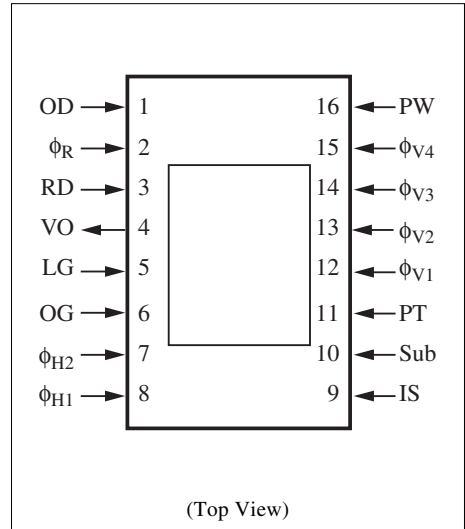
### ■ Features

- Effective pixel number 771 (horizontal) × 492 (vertical)
- High sensitivity
- Broad dynamic range
- Low smear
- Electronic shutter

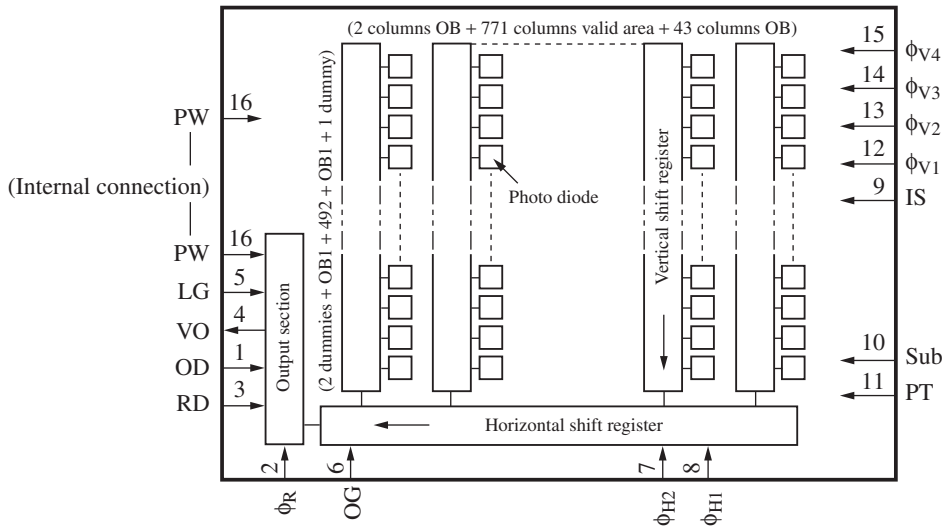
### ■ Applications

- Surveillance cameras
- FA, OA cameras

### ■ Pin Assignments



■ Block Diagram



■ Pin Descriptions

| Pin No. | Symbol      | Description                       | Pin No. | Symbol      | Description                           |
|---------|-------------|-----------------------------------|---------|-------------|---------------------------------------|
| 1       | OD          | Output drain                      | 9       | IS          | Horizontal CCD input source           |
| 2       | $\phi_R$    | Reset pulse                       | 10      | Sub         | Substrate                             |
| 3       | RD          | Reset drain                       | 11      | PT          | P-well for protection circuit         |
| 4       | VO          | Video output                      | 12      | $\phi_{V1}$ | Vertical shift register clock pulse 1 |
| 5       | LG          | Output load transistor gate       | 13      | $\phi_{V2}$ | Vertical shift register clock pulse 2 |
| 6       | OG          | Output gate                       | 14      | $\phi_{V3}$ | Vertical shift register clock pulse 3 |
| 7       | $\phi_{H2}$ | Horizontal register clock pulse 2 | 15      | $\phi_{V4}$ | Vertical shift register clock pulse 4 |
| 8       | $\phi_{H1}$ | Horizontal register clock pulse 1 | 16      | PW          | P-well                                |

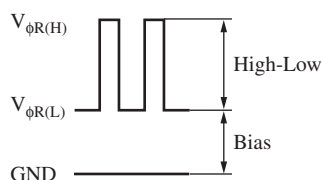
■ Device Parameter (H × V)

| Parameter                     | Value       | Unit            |
|-------------------------------|-------------|-----------------|
| Total pixel number            | 816 × 495   | pixel           |
| Effective pixel number        | 771 × 492   | pixel           |
| Active pixel number           | 759 × 482   | pixel           |
| Image sensing block dimension | 4.93 × 3.69 | mm <sup>2</sup> |
| Pixel dimension               | 6.40 × 7.50 | $\mu\text{m}^2$ |

## ■ Absolute Maximum Ratings and Operating Conditions

| Parameter             | Absolute maximum rating |             | Operating condition   |                       |      | Unit |   |
|-----------------------|-------------------------|-------------|-----------------------|-----------------------|------|------|---|
|                       | Lower limit             | Upper limit | Min                   | Typ                   | Max  |      |   |
| $V_{RD}$              | -0.2                    | 18.0        | 14.5                  | 15.0                  | 15.5 | V    |   |
| $V_{OD}$              | -0.2                    | 18.0        | 14.5                  | 15.0                  | 15.5 | V    |   |
| $V_{IS}$              | -0.2                    | 18.0        | 14.5                  | 15.0                  | 15.5 | V    |   |
| $V_{LG}$              | (Internal bias)         |             |                       |                       |      | V    |   |
| $V_{OG}$              | (Internal bias)         |             |                       |                       |      | V    |   |
| $V_{PT}^{*3,4}$       | -9.0                    | 0.2         | -7.3                  | -7.0                  | -6.7 | V    |   |
| $V_{PW}$              | (Reference voltage)     |             | —                     | 0                     | —    | V    |   |
| $V_{\phi R}^{*1}$     | High-Low                | -0.2        | 5.0                   | 3.0                   | 3.3  | 3.6  | V |
|                       | Bias                    | -0.2        | 5.0                   | (Supplied internally) |      |      | V |
| $V_{\phi H1}$         | High                    | -0.2        | 5.0                   | 3.0                   | 3.3  | 3.6  | V |
|                       | Low                     | -0.2        | 5.0                   | -0.1                  | 0    | 0.1  | V |
| $V_{\phi H2}$         | High                    | -0.2        | 5.0                   | 3.0                   | 3.3  | 3.6  | V |
|                       | Low                     | -0.2        | 5.0                   | -0.1                  | 0    | 0.1  | V |
| $V_{Sub}^{*2}$        | -0.2                    | 45.0        | (Supplied internally) |                       |      | V    |   |
| $\phi V_{Sub}^{*2}$   | -0.2                    | 45.0        | 21.0                  | 22.0                  | 23.0 | V    |   |
| $V_{\phi V1}^{*3,4}$  | High                    | -9.0        | 18.0                  | 14.5                  | 15.0 | 15.5 | V |
|                       | Middle                  | -9.0        | 18.0                  | -0.2                  | 0    | 0.2  | V |
|                       | Low                     | -9.0        | 18.0                  | -7.3                  | -7.0 | -6.7 | V |
| $V_{\phi V2}^{*3,4}$  | Middle                  | -9.0        | 15.0                  | -0.2                  | 0    | 0.2  | V |
|                       | Low                     | -9.0        | 15.0                  | -7.3                  | -7.0 | -6.7 | V |
| $V_{\phi V3}^{*3,4}$  | High                    | -9.0        | 18.0                  | 14.5                  | 15.0 | 15.5 | V |
|                       | Middle                  | -9.0        | 18.0                  | -0.2                  | 0    | 0.2  | V |
|                       | Low                     | -9.0        | 18.0                  | -7.3                  | -7.0 | -6.7 | V |
| $V_{\phi V4}^{*3,4}$  | Middle                  | -9.0        | 15.0                  | -0.2                  | 0    | 0.2  | V |
|                       | Low                     | -9.0        | 15.0                  | -7.3                  | -7.0 | -6.7 | V |
| Operating temperature | -10                     | 70          | —                     | 25                    | —    | °C   |   |
| Storage temperature   | -30                     | 80          | —                     | —                     | —    | °C   |   |

Note) \*1 : Reset



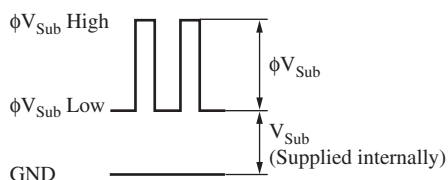
\*3: Absolute maximum rating  $-0.2 < V_{\phi V} - V_{PT} < 24.5$  (V)

\*4: Relation between  $V_{PT}$  and  $V_{\phi VL}$

Set  $V_{PT}$  that is to meet the following conditions for VL voltage of the vertical shift clock waveform.

$$V_{PT} \leq VL \quad (V_{\phi V1L} \text{ to } V_{\phi V4L})$$

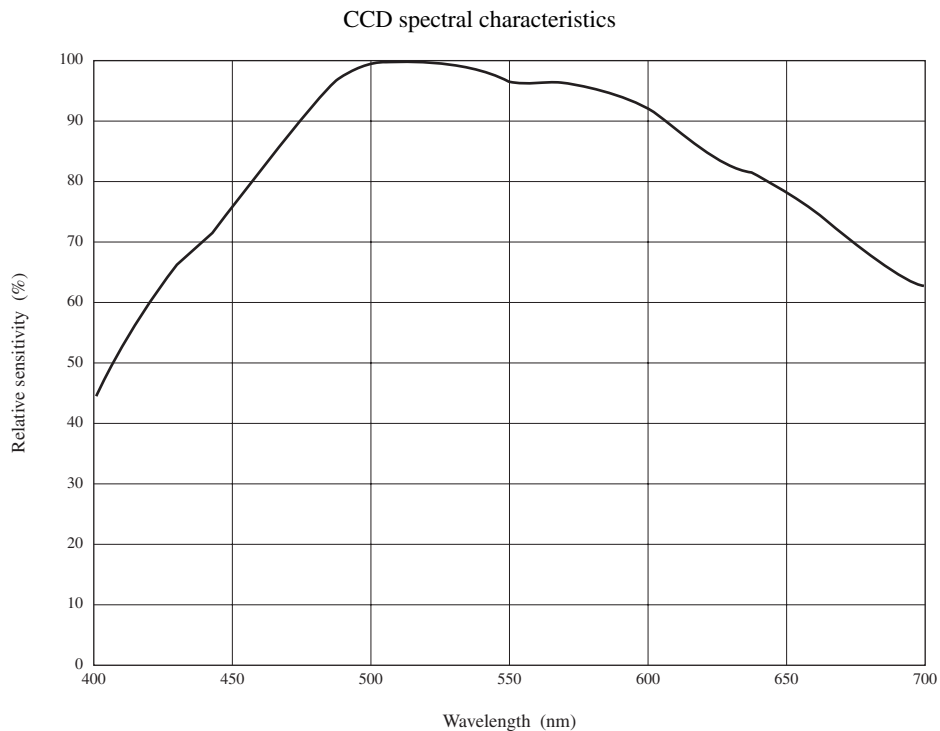
\*2:  $V_{Sub}$  when using electronic shutter function



■ Optical Characteristics

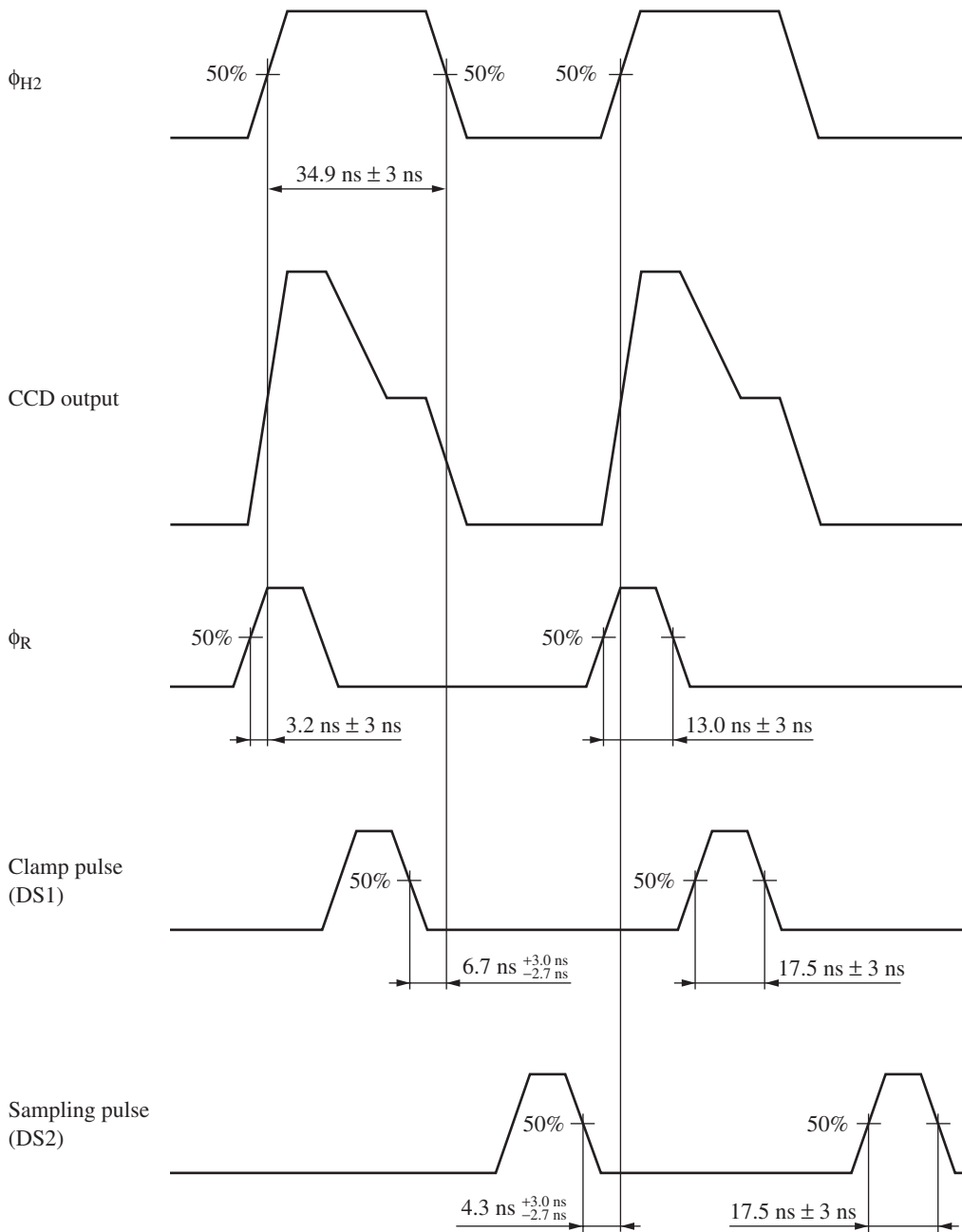
| Parameter                 | Symbol | Conditions                   | Min | Typ  | Max | Unit |
|---------------------------|--------|------------------------------|-----|------|-----|------|
| S/N ratio (dark)          | S/Nd   | Dark condition               | 57  | 60   | —   | dB   |
| Sensitivity               | So     | Standard condition (J chart) |     | 750  | —   | mV   |
| Carrier saturation output | Sa     | J chart                      |     | 1400 | —   | mV   |
| Vertical smear            | Sm     | 1/10 V chart, F2.8           | —   | -100 | -95 | dB   |

■ Graph of Characteristics



■ Timing Diagram

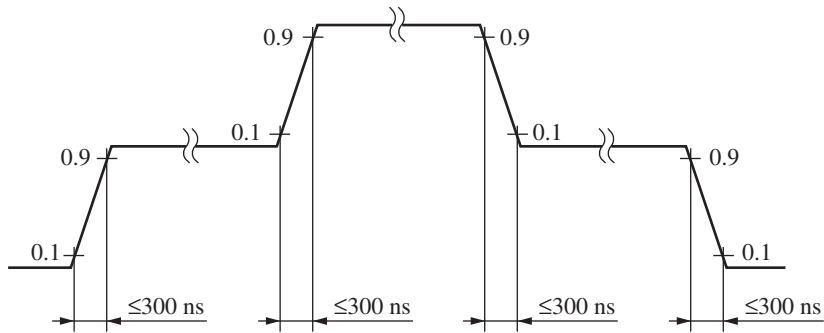
- High speed pulse timing



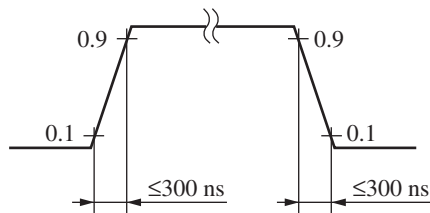
■ Timing Diagram (continued)

- Rise time and fall time of each pulse

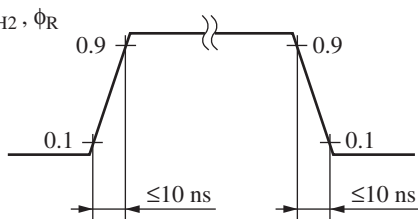
$\phi_{V1}, \phi_{V3}$



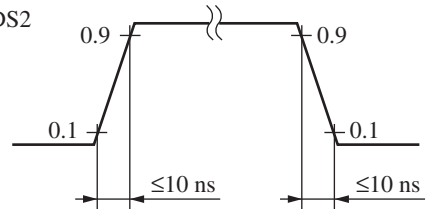
$\phi_{V2}, \phi_{V4}$



$\phi_{H1}, \phi_{H2}, \phi_R$

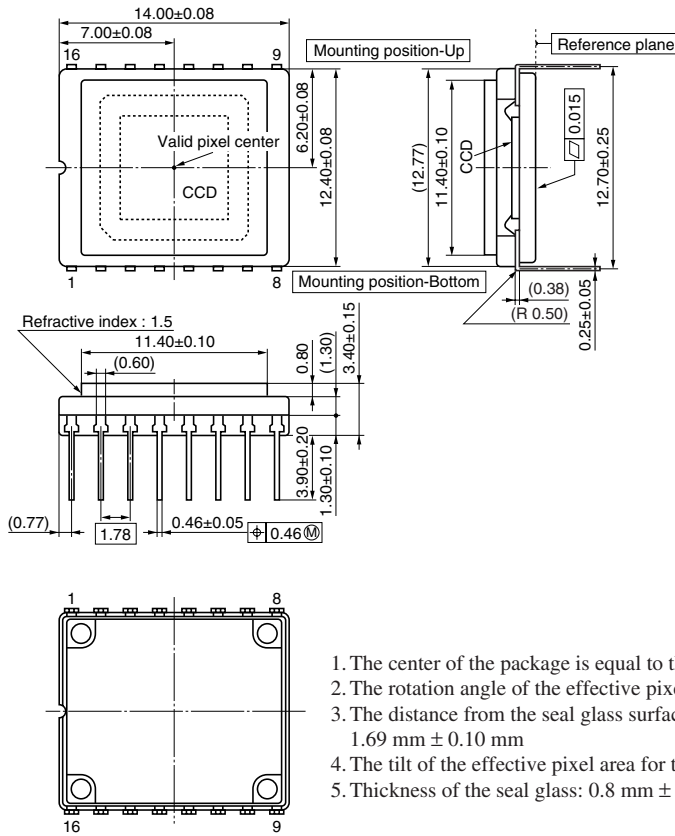


DS1, DS2



■ Package Dimensions (unit: mm)

• WDIP016-P-0500C



1. The center of the package is equal to the center of the effective pixel area.
2. The rotation angle of the effective pixel area: up to  $\pm 1.0$  degree
3. The distance from the seal glass surface to the surface of the effective pixel area:  $1.69 \text{ mm} \pm 0.10 \text{ mm}$
4. The tilt of the effective pixel area for the seal glass surface: up to  $30 \mu\text{m}$
5. Thickness of the seal glass:  $0.8 \text{ mm} \pm 0.10 \text{ mm}$ , and the refractive index: 1.50

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